AD Combo Module Kit User's Manual

D000003 Rev C

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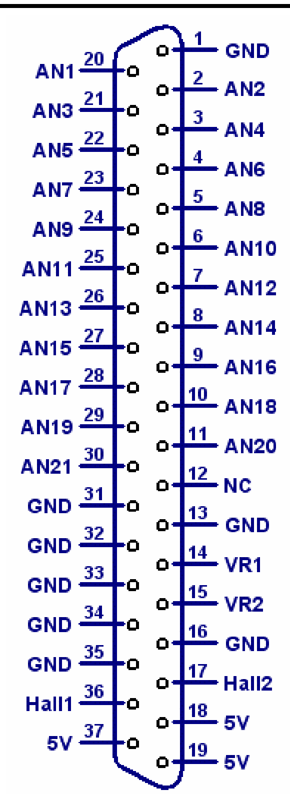
Introduction

The Drivven cRIO AD Combo Module Kit offers a set of automotive-style analog and digital inputs to interface with standard automotive sensors.

Features:

- 21 Ch. Analog inputs
  - 12-bit A/D Converter
  - 4 ksps per channel
  - Optional pullup, pulldown, and divide resistors
  - Anti-aliasing filter per channel
  - Short circuit protection
  - Dedicated 2.5V precision reference
- 2 Ch. VR sensor inputs
  - +/-150V input range
  - Adaptive threshold
- 2 Ch. Hall-effect sensor or general purpose digital inputs
  - Digital input with hysteresis
  - Short circuit protection
  - Optional pullup, pulldown, and divide resistors
  - Analog filter for noise rejection
- Sensor power output
  - 5V @ 100mA

Pinout



Hardware

This module provides analog inputs, VR sensor inputs and hall-effect sensor inputs. It also provides sensor power and ground. Sensor power is provided directly from the cRIO chassis backplane. Sensors should not draw more than a total of 100mA.

A properly strain relieved DB-37 connector (not included) is used to interface to the module. National Instruments provides the "cRIO-9933 37-pin Conn. Kit, screw term conn. and DSUB shell" which is compatible with this module. However, any DB-37 connector system may be used.

Analog Inputs

All analog inputs are similar to production automotive ECU analog inputs. They are single ended inputs and provide filtering and short circuit protection.
For best results, the power and ground of the sensors should be provided by this module.
A pullup or pulldown is recommended for every input in order to facilitate open/defective sensor faults. These are provided with the standard configuration.

Standard Channel Configuration

Generic Analog Input Circuit

Figure 1 shows the generic schematic representation of all analog inputs. An AD Combo module having a standard configuration will have a mixture of channel configurations according to the circuits described below.

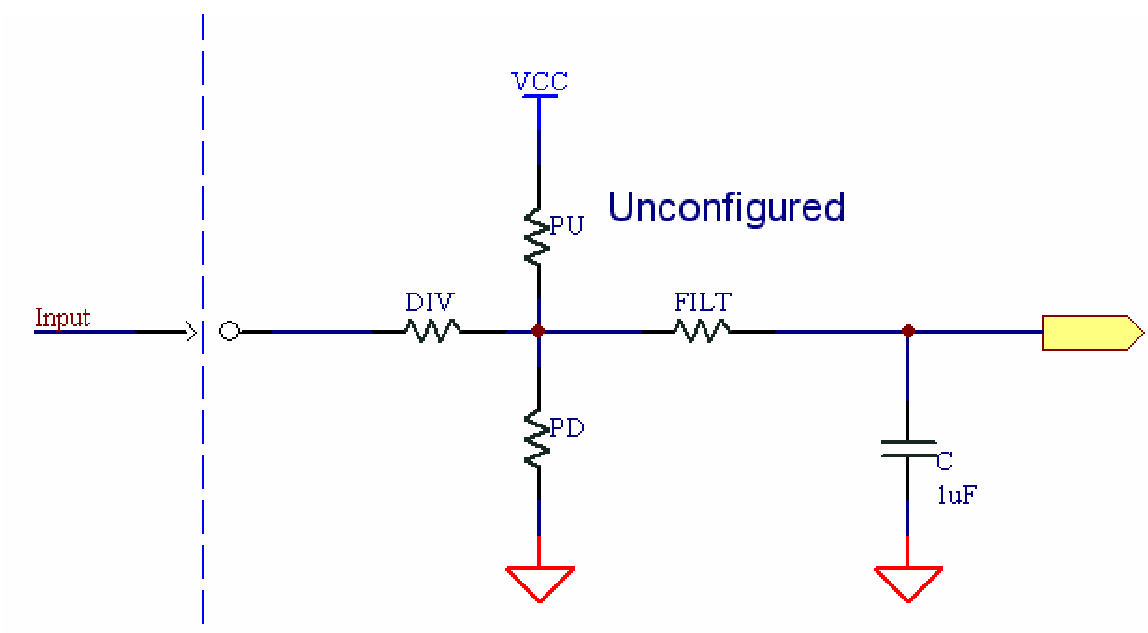


Figure 1. Unconfigured generic analog input circuit schematic

Divided Inputs

Figure 2 shows the analog input circuit configuration for measuring voltages from 0 to 33 V. This is standard configuration for channels 1 - 3.

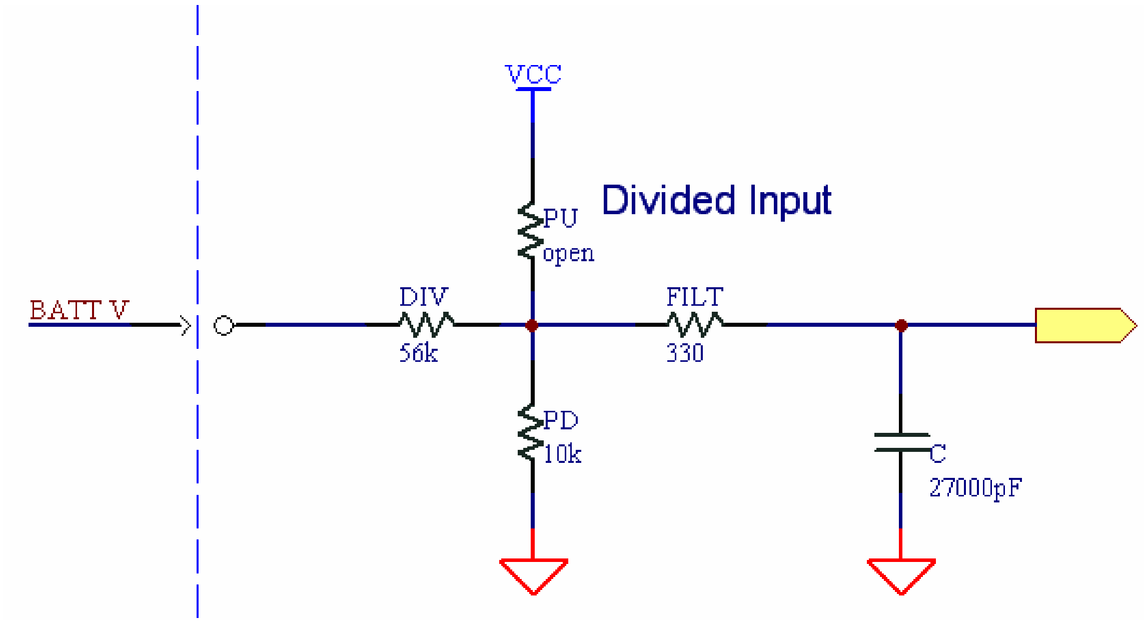


Figure 2. Analog input configuration for 0 to 33 V inputs.

Active Inputs / Potentiometer Inputs

Figure 3 shows the analog input circuit configuration for both active-drive analog sensors and potentiometers. This is the standard configuration for channels 4 - 16.

This circuit utilizes a weak pulldown for open circuit detection. If the channel is connected to a potentiometer, the pulldown will slightly modify the voltage seen by the A/D converter, as compared to an input circuit without the pulldown. Therefore, a full potentiometer calibration must be performed since the voltage from this circuit will not readily correlate to the voltage resulting from no pulldown.

Examples of potentiometers are throttle position and pedal position sensors.

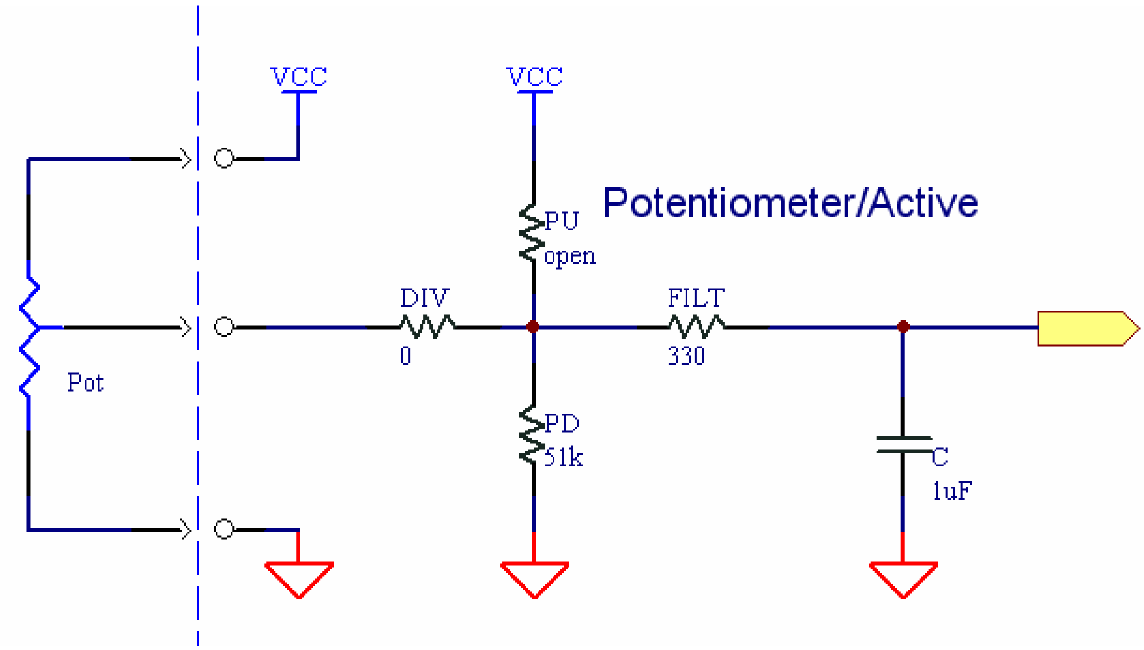


Figure 3. Analog input configuration for active sensors and potentiometers

Thermistor Inputs / Switch Inputs

Figure 4 shows the analog input circuit configuration for thermistors and switches. This is standard configuration for channels 18 - 21.

Thermistor inputs have a strong pullup to create a voltage divider with the sensor. Refer to the sensor datasheet for sensor resistance curves. Most production automotive temperature sensors are thermistors which have a maximum cold resistance of approximately 100 Kohms and a resistance of approximately 100 ohms at 150 degrees C. The pullup resistor of 1 Kohms will provide a useable output voltage range for thermistors of this type.

When used as a switch input, the switch should short to ground when it is closed.

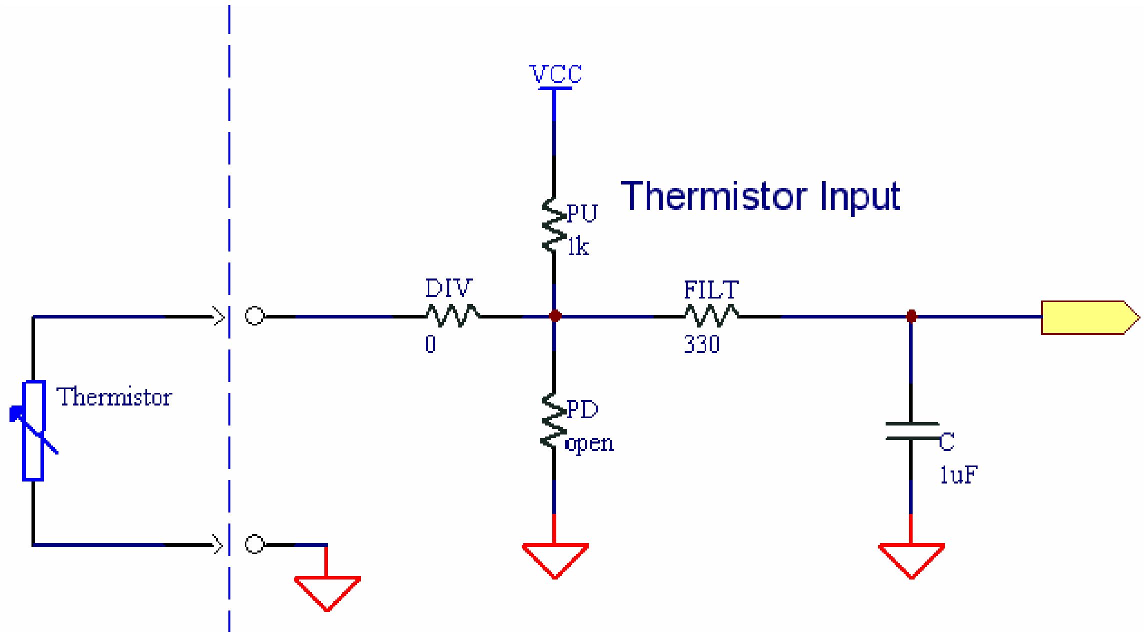


Figure 4. Analog input configuration for thermistors and switches

VR Sensor Inputs

The AD Combo module provides two identical VR sensor inputs. A Variable Reluctance (VR) sensor input is a standard low cost automotive speed sensing input. It is an electro-magnetic sensing device containing a winding of wire around a permanent magnetic core. It relies on the movement of ferrous material (steel teeth) past the tip of the sensor to change the magnetic flux of the sensor. This creates a voltage pulse across the leads of the sensor's wire coil. Figures 7 and 8 below show a typical VR signal with respect to toothed wheels, as shown in figures 5 and 6. The VR signal will go positive as a tooth approaches the sensor tip. The signal will then rapidly swing back through zero precisely at the center of the tooth. As the tooth moves away from the sensor tip the voltage will continue in the negative direction and then return to zero.

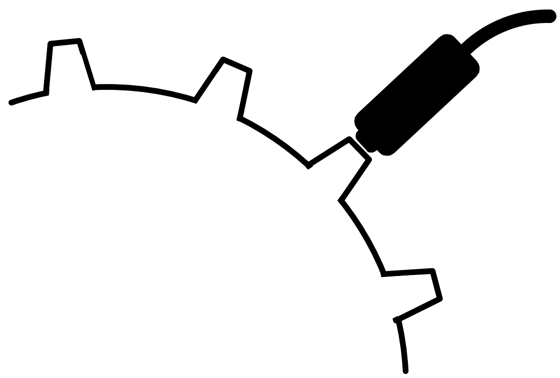


Figure 5. Positive tooth trigger wheel

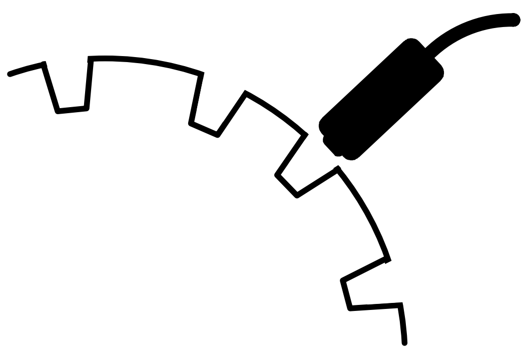


Figure 6. Negative tooth trigger wheel

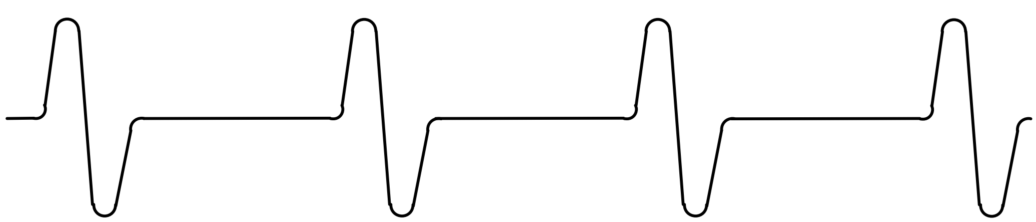


Figure 7. Correct signal polarity for VR input circuit

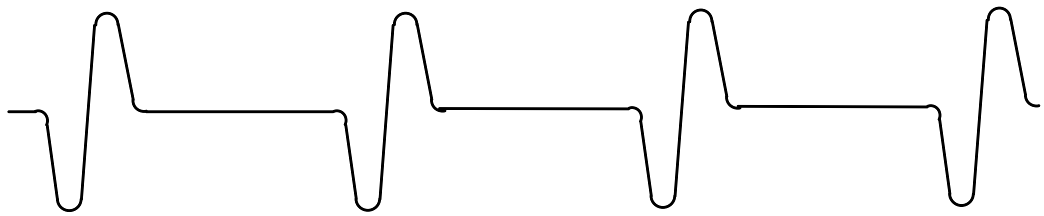


Figure 8. Incorrect signal polarity for VR input circuit

Each VR sensor input requires two connections. The AD Combo module pins labeled VR1 and VR2 are the positive sensor inputs. The negative sensor inputs must be connected to GND pins on the module. The polarity of the sensor connection to the module is critical. The leads of the sensor should be connected such that the positive input of the VR circuit sees the waveform shown in Figure 7. The waveform shown Figure 8 is incorrect, and the VR circuit will not properly respond to this waveform. The rapid zero crossing of the VR signal must be in the negative direction.

The polarity of the physical tooth or gap on the trigger wheel will contribute to the polarity of the voltage pulse from the sensor. Figure 5 demonstrates a positive physical tooth polarity and Figure 6 demonstrates a negative physical tooth polarity. Assuming the lead polarity of a sensor remained the same, one of the configurations would generate the waveform shown in Figure 7, while the other configuration would generate the waveform shown in Figure 8.

Triggers wheels are designed so that the physical center of each tooth or gap corresponds to a known angular position of the wheel. This physical center of the tooth or gap always corresponds to the rapid zero-crossing of the generated voltage pulse.

The VR circuit is designed so that the rapid negative zero-crossing of the raw sensor signal corresponds to the rising edge of a 50 microsecond one-shot output to the RIO FPGA. An example of this is shown in Figure 9. Within LabVIEW FPGA the system designer can route this digital signal to the EPT CrankSig or CamSig input. The signal can also be routed to any other speed measurement sub-VI.

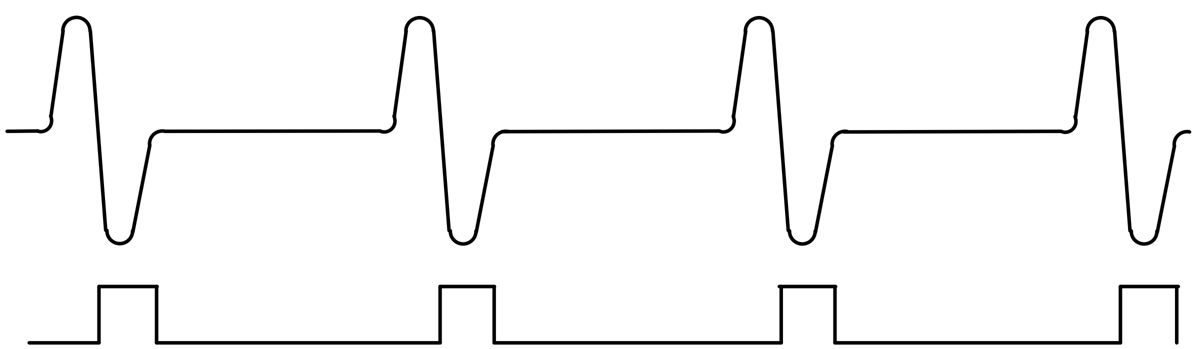


Figure 9. VR input pulse and resulting digital output from VR circuit

The absolute maximum VR pulse amplitude allowed by the circuit is +/-150 volts. If the input signal exceeds this voltage, damage may occur to the circuit. The amplitude should not exceed +/-150 volts at maximum engine speed. The minimum VR pulse amplitude that will generate a digital output by the VR circuit is +/-100 millivolts.

The VR circuit implements adaptive noise rejection features during continuous incoming VR pulses. In general, an adaptive arming threshold voltage is generated with each VR pulse and bleeds down thereafter. The next pulse must have an amplitude that exceeds the arming threshold in order for a digital output to be generated at the rapid zero-crossing. The initial arming threshold is set to approximately 70% of each pulse's amplitude.

Given a constant gap between the sensor and the trigger teeth, the amplitude of a VR pulse is directly proportional to the speed of the trigger wheel. For example, if the VR amplitude at 1000 RPM is +/-10 volts, then the amplitude at 2000 RPM will be +/-20 volts. By using an oscilloscope to measure the VR amplitude at a low speed, this relationship can be used to determine what the maximum amplitude will be at the maximum speed. If the maximum amplitude of +/-150 volts will be exceeded at maximum speed, then the sensor gap must be increased, or the designer must obtain a custom VR circuit configuration from Drivven.

Hall-Effect Sensor Inputs

The AD Combo module provides two identical hall-effect sensor input circuits. The hall-effect inputs are designed to take a digital input from a hall-effect or proximity sensor. Typical sensors of this type will have an open-collector output, requiring a pullup resistor at the collector. The hall-effect inputs will also read active TTL compatible signals. The standard configuration includes a 4.7K pullup to 5V for use with open collector type inputs. The input is protected against typical automotive battery voltages and can be connected to actively-driven, battery voltage signals.

The circuit's output to the RIO FPGA reverses the polarity of the input by going low when the input voltage is greater than 3.6V. The output goes high when the input is less than 1.4V. The input hysteresis requires the input to move all the way to the opposite logic level before the output changes.

Figure 10 show the standard configuration of the hall-effect sensor input circuits.

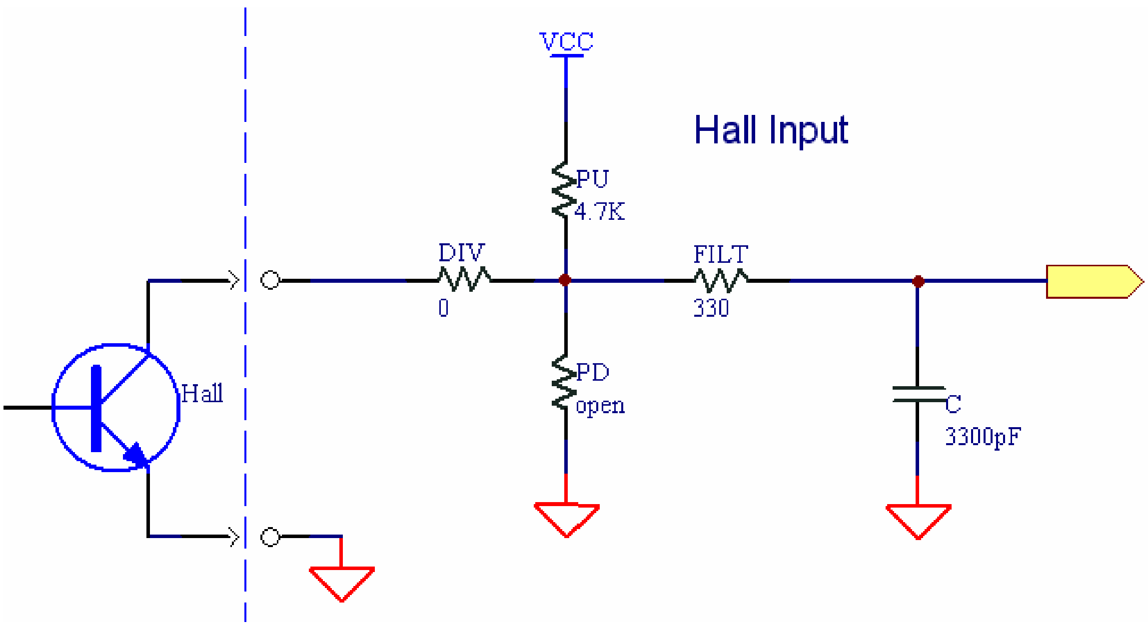


Figure 10. Hall-effect circuit input configuration

Software

The AD Combo Module Kit is provided with a LabVIEW FPGA VI for interfacing to the module and reporting analog, VR and hall signal results.

Figure 11 shows the icon which represents ad_combo.vi.

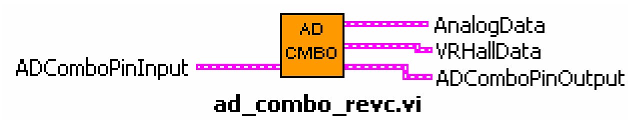


Figure 11. AD Combo VI icon with leads.

VERY IMPORTANT NOTES:
The VR/Hall VI requires:

- LabVIEW 7.1 or later
- LabVIEW FPGA Module 1.1 or later
- NI-RIO 1.1 or later

The AD Combo VI must be placed within a Single Cycle Loop (SCL) of a LabVIEW FPGA block diagram. The SCL must execute at the default clock rate of 40 MHz.

The AD Combo VI requires a pre-synthesized netlist file having a matching name and an extension of .ngc. The netlist file must be located in the same directory as the VI.

The AD Combo VI requires the installation of a special CompactRIO module support package called cRIO-generic. Please follow the steps below to install the cRIO-generic package:

1. Confirm that LabVIEW is closed.
2. Add the line **`cRIO_FavoriteBrand=generic`** to the LabVIEW INI file. The LabVIEW INI file is typically found at C:\Program Files\National Instruments\LabVIEW 7.1\LabVIEW.ini.
3. Upon restarting LabVIEW, the cRIO-generic module will appear in the list of available modules within the LabVIEW FPGA cRIO configuration dialog. The cRIO configuration dialog is presented while configuring FPGA I/O pins.

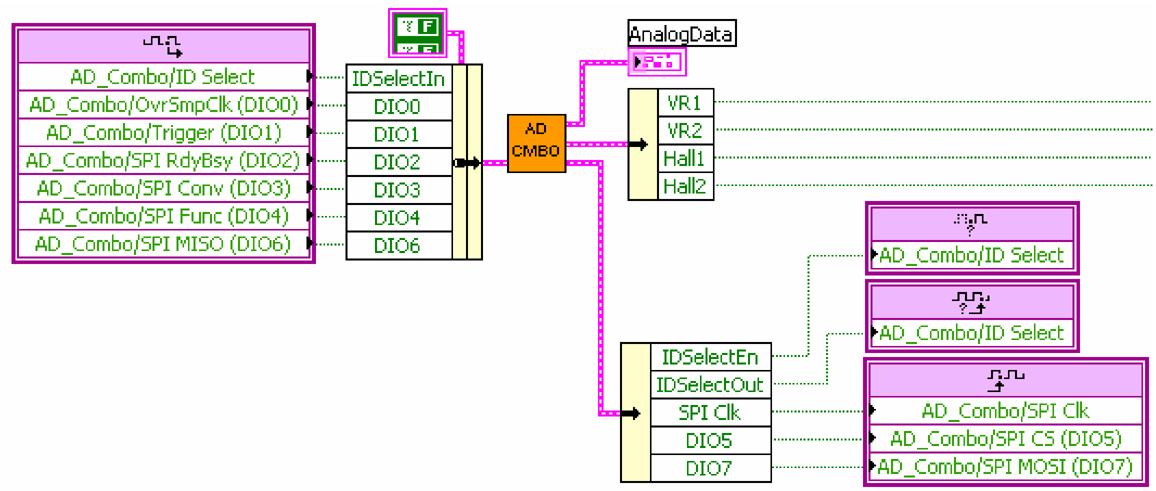
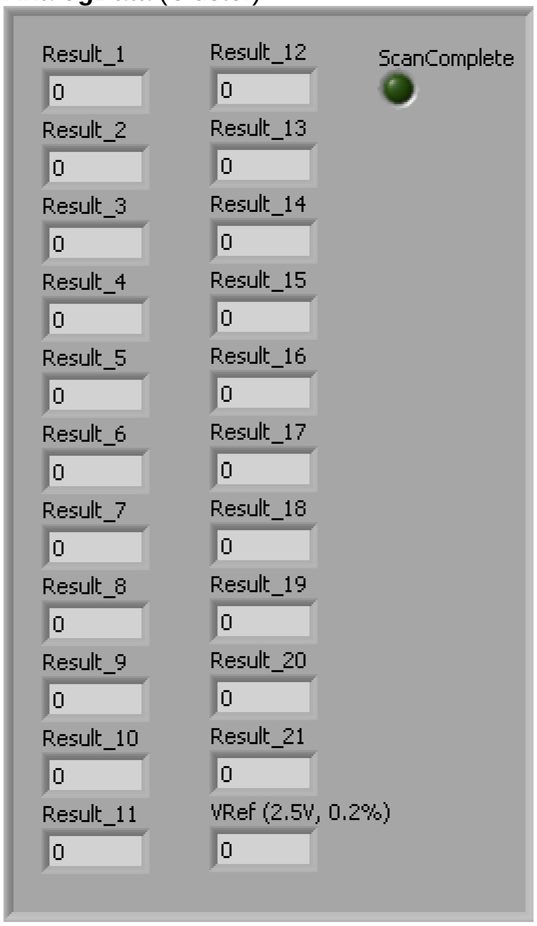


Figure 12. Example block diagram implementation of ad_combo.vi.

ADComboPinInput (Cluster)
The ADComboPinInput cluster contains seven boolean controls which must be connected to their corresponding cRIO I/O pin using a Digital Input function.

ADComboPinOutput (Cluster)
The ADComboPinOutput cluster contains five boolean indicators which must be connected to their corresponding cRIO I/O pins. The boolean indicator named IDSelectEn must be connected using a Digital Enable function. The boolean indicator named IDSelectOut must be connected using a Digital Data function. The remaining boolean indicators must be connected using a Digital Output function.

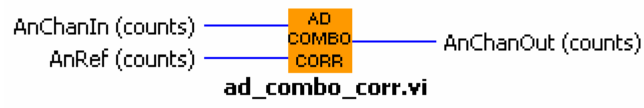
AnalogData (Cluster)



Result_X (int16): The analog to digital conversion result in terms of 12-bit A/D counts from 0 to 4095, corresponding to 0 to 5V.

VRef (2.5V, 0.2%): The AD Combo uses a high reference of 5.0V +/-5% for it A/D converters. Since +/-5% may not be an adequate precision for some measurements, one channel of the AD Combo measures a reference of 2.5V +/-0.2%. The reference value can be used to correct other channels when it is necessary to have a more precise absolute voltage measurement. For channels which are measuring ratiometric signals, such as potentiometers, this correction is not needed.

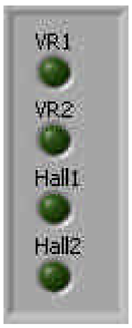
A VI named ad_combo_corr.vi is provided with the kit to perform this correction at the windows or RT level.



The A/D counts of AD Combo channel "VRef" should be wired to the AnRef (counts) input. The A/D counts of the channel to be corrected should be connected to the AnChanIn (counts) input. The absolute, corrected A/D counts are output on AnChanOut (counts). This correction assumes a 12-bit A/D converter and a nominal reference of 2.5V. This VI should be instantiated at the Windows or RT level, not within the FPGA.

ScanComplete (boolean): A 40 MHz one-clock one-shot output indicating that all channel registers have been updated once. This output may be used for filtering purposes within the RIO FPGA. ScanComplete one-shot will be asserted at the rate of 4000 Hz.

VRHallData (Cluster)



VRX (boolean): The VR output signal will go TRUE at the rapid negative zero crossing of the external VR pulse and remain TRUE for approximately 50 microseconds.

HallX (boolean): The Hall output is an inverted and filtered version of the external signal presented to the hall-effect input channel.

Standard Circuit Configuration

The AD Combo module is hardware-configurable. It may be ordered with the default options outlined below or may be custom ordered. Additionally, it may be configured by the user. However, this procedure is only recommended for users highly skilled in circuit board rework due to the small surface mount parts involved.

Standard Analog Configuration

Channel	Pullup Resistor (ohms)	Pulldown Resistor (ohms)	Divide Resistor (ohms)	Break Frequency (Hz)	Intended Use
1	open	10k	56k	500	33V Measurment
2	open	10k	56k	500	33V Measurment
3	open	10k	56k	500	33V Measurment
4	open	51k	0	500	Active / Pot
5	open	51k	0	500	Active / Pot
6	open	51k	0	500	Active / Pot
7	open	51k	0	500	Active / Pot
8	open	51k	0	500	Active / Pot
9	open	51k	0	500	Active / Pot
10	open	51k	0	500	Active / Pot
11	open	51k	0	500	Active / Pot
12	open	51k	0	500	Active / Pot
13	open	51k	0	500	Active / Pot
14	open	51k	0	500	Active / Pot
15	open	51k	0	500	Active / Pot
16	open	51k	0	500	Active / Pot
17	1k	open	0	500	Thermistor / Switch
18	1k	open	0	500	Thermistor / Switch
19	1k	open	0	500	Thermistor / Switch
20	1k	open	0	500	Thermistor / Switch
21	1k	open	0	500	Thermistor / Switch
22	2.5 Volt (0.2%) Precision Reference				

Standard VR Configuration

Channel	VR Amplitude Voltage
1	+/- 150V
2	+/- 150V

Standard Hall Configuration

Channel	Pullup Resistor (ohms)	Pulldown Resistor (ohms)	Divide Resistor (ohms)	Break Frequency (Hz)	Intended Use
1	4.7k	open	0	150K	Hall, Prox, Switch or TTL
2	4.7k	open	0	150K	Hall, Prox, Switch or TTL

Custom Configuration

For an additional service charge, Drivven will custom configure each analog, VR and Hall channel. Customization can take place during or after module purchase.

It is possible for the customer to configure the channels. All user serviceable parts are on the bottom of the board and their locations are shown in figure 13. To change the analog or hall circuit configuration, use the resistor-type and channel-number grid headings on the top and sides, respectively, to locate the component you wish to change. The VR Limit resistor can be configured to change the maximum amplitude voltage setting as follows:

Resistance = MaxAmplitude / 0.003

The VR Adapt location should not be modified.

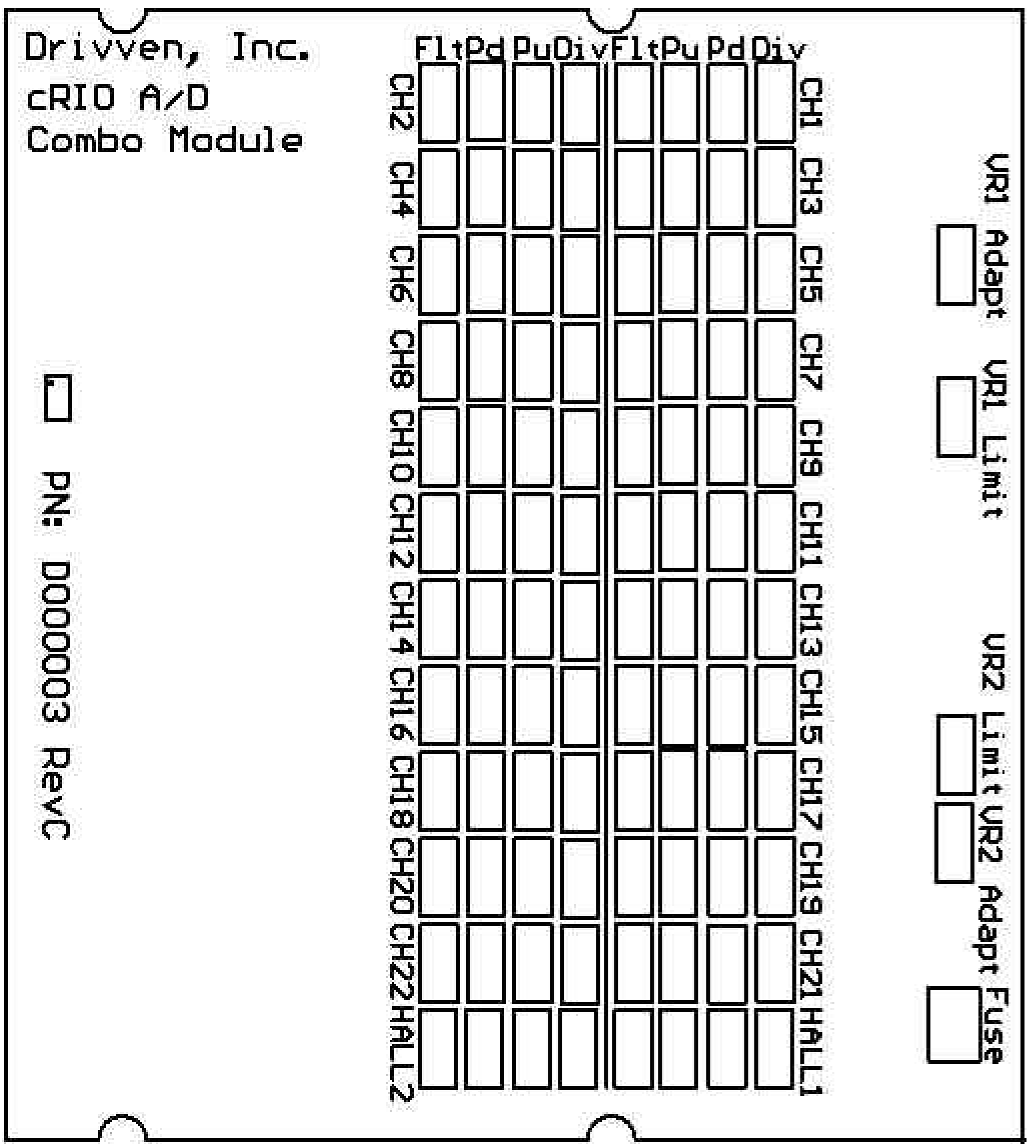


Figure 13. Bottom side of AD Combo module showing serviceable parts.

When requesting a custom configuration, please provide all of the following information.

Customer Business Name	
Contact Name	
Contact Phone	
Contact Email	
Shipping Address	
Unit Serial Number	
Has this unit been modified by the user?	

Channel	Pullup Resistor (ohms)	Pulldown Resistor (ohms)	Divide Resistor (ohms)	Break Frequency (Hz)	Intended Use
Analog 1					
Analog 2					
Analog 3					
Analog 4					
Analog 5					
Analog 6					
Analog 7					
Analog 8					
Analog 9					
Analog 10					
Analog 11					
Analog 12					
Analog 13					
Analog 14					
Analog 15					
Analog 16					
Analog 17					
Analog 18					
Analog 19					
Analog 20					
Analog 21					
Hall 1					
Hall 2					

Channel	VR Amplitude Voltage
VR 1	
VR 2	

Examples

The following screen capture in figures14 shows a LabVIEW FPGA block diagram with the AD Combo VI used for general purpose analog and speed measurement. This FPGA application is entirely contained within a single cycle loop, clocked at the required 40 MHz. The PinInput and PinOutput clusters are wired to LabVIEW FPGA I/O pins which are configured for a cRIO controller chassis or a cRIO R-Series expansion chassis. Refer to the LabVIEW FPGA documentation for details about configuring cRIO I/O pins.

This example makes all of the cluster controls and indicators available to the front panel, and therefore available to the CPU program. If some of the controls within clusters are to be constants and do not need to be made available to the CPU, then cluster bundle and unbundle functions should be used to wire in constants. This will save FPGA resources by limiting the number of visible controls to only those that are necessary at the CPU level.

This example VI is included in the AD Combo Module Kit VI software bundle.

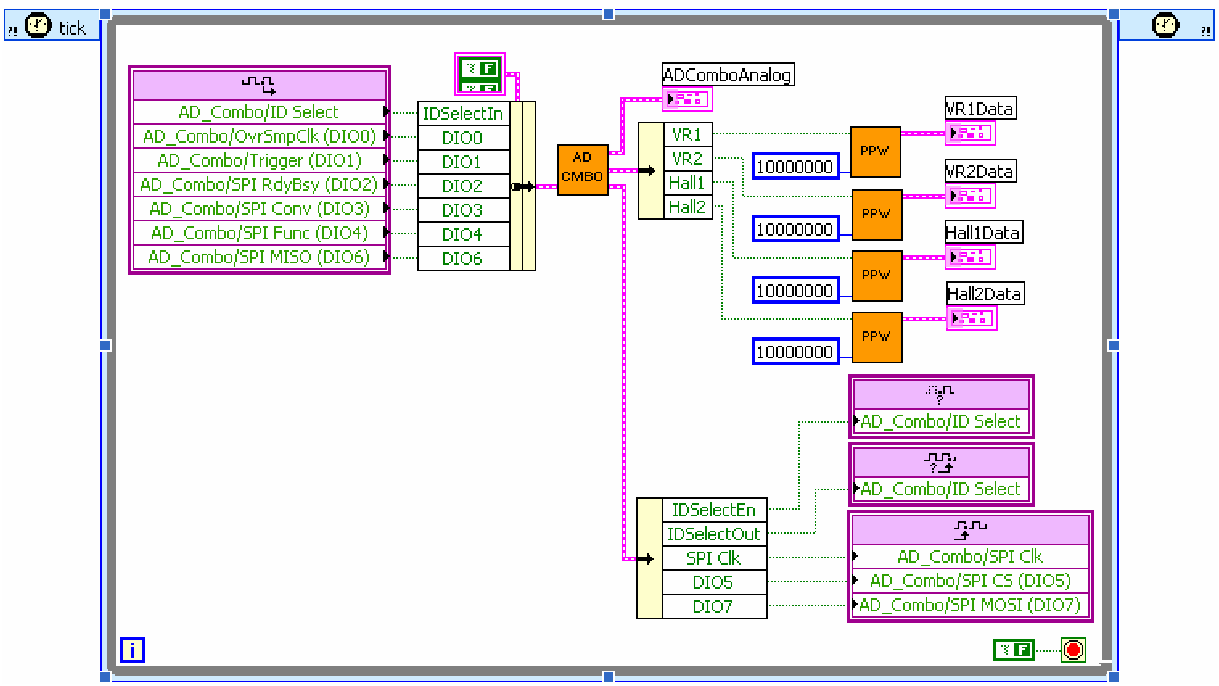


Figure 14. LabVIEW FPGA Block diagram example of ad_combo.vi used as general purpose analog and speed measurement.