General FPGA VIs
Documentation
RevA

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Drivven ,Inc. • 12001 Network Blvd, Bldg E, Suite 110 • San Antonio, Texas 78249 • USA
Phone : 210.248.9308
Web : www.drivven.com , E-mail : info@drivven.com

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Introduction

Each Drivven software toolkit installation includes a tool palette group called General FPGA VIs. This group includes several sub VIs which can assist with manipulating and filtering Boolean signals. Below are the documentation of each sub VI.

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filt_int_reva.vi

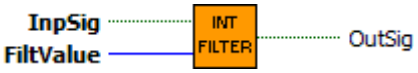
This VI filters a Boolean signal using an integrating algorithm. When the Boolean signal changes states, an internal timer resets. When the timer reaches the value specified by FiltValue, then the input Boolean state passes through to the output.

This function effectively filters out positive or negative glitches which are smaller than FiltValue. FiltValue is specified in terms of clock ticks.

This VI must be placed within a Single Cycle Loop (SCL) of a LabVIEW FPGA block diagram.

The FPGA VI requires a pre-synthesized netlist file having a matching name and an extension of .ngc. The netlist file must be located in the same directory as the matching VI. The installer will place this file in the LabVIEW addons directory along with the FPGA VI.

Connector Pane



Controls and Indicators

InpSig Input Boolean signal to be filtered.

FiltValue Positive or negative signal glitches smaller than FiltValue will be rejected. FiltValue is specified in terms of clock ticks.

OutSig Filtered output signal.

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one_shot_s1_reva.vi

This VI takes a Boolean Input and generates a one-clock-period one-shot pulse upon the rising edge of Input. The clock period of the FPGA design determines the pulsewidth of the one-shot. The default clock rate of LabVIEW FPGA is 40MHz.

This VI must be placed within a Single Cycle Loop (SCL) of a LabVIEW FPGA block diagram.

The FPGA VI requires a pre-synthesized netlist file having a matching name and an extension of .ngc. The netlist file must be located in the same directory as the matching VI. The installer will place this file in the LabVIEW addons directory along with the FPGA VI.

Connector Pane

Controls and Indicators

Input Input for generating the one-shot output pulse.

Output One-shot output pulse.

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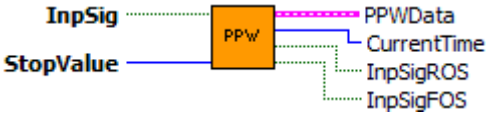
ppw_reva.vi

This VI measures the period and pulse width of an incoming Boolean signal (InpSig). StopValue is the specified maximum number of clock ticks between InpSig rising edges at which the measured Period will be reported as zero. One-shots are generated at the rising and falling edges of the input which can be used to trigger further processing upon either signal edge.

This VI must be placed within a Single Cycle Loop (SCL) of a LabVIEW FPGA block diagram.

The FPGA VI requires a pre-synthesized netlist file having a matching name and an extension of .ngc. The netlist file must be located in the same directory as the matching VI. The installer will place this file in the LabVIEW addons directory along with the FPGA VI.

Connector Pane



Controls and Indicators

InpSig Signal to be measured for period and pulse width.

StopValue When CurrentTime reaches StopValue, then Stopped is set to TRUE, and Period and PulseWidth are set to zero.

PPWData Cluster of data reporting the measured period and pulse width of the incoming InpSig.

- **Period** Period between the most recent rising edges of InpSig in terms of clock ticks. Period is reported as zero when Stopped is TRUE.
- **PulseWidth** Pulse width from the most recent rising edge to the most recent falling edge of InpSig in terms of clock ticks. PulseWidth is reported as zero when Stopped is TRUE.
- **Stopped** Set to TRUE when StopValue is reached by CurrentTime.

CurrentTime Running clock ticks since the most recent rising edge of InpSig.

InpSigROS Rising-edge one-clock one-shot of InpSig.

InpSigFOS Falling-edge one-clock one-shot of InpSig.

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ppwa_reva.vi

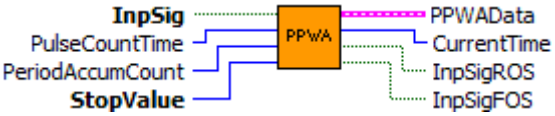
This VI reports the following from InpSig:
1.) Period of an input pulse train, rising to rising edge.
2.) Positive pulse width.
3.) Accumulates period over a specified number of pulses.
4.) Counts pulses over a specified period of time.
5.) Outputs 0 for all results and asserts Stopped if CurrentTime exceeds StopValue.

StopValue is the specified maximum number of clock ticks between InpSig rising edges at which the measured Period will be reported as zero. One-shots are generated at the rising and falling edges of the input which can be used to trigger further processing upon either signal edge.

This VI must be placed within a Single Cycle Loop (SCL) of a LabVIEW FPGA block diagram.

The FPGA VI requires a pre-synthesized netlist file having a matching name and an extension of .ngc. The netlist file must be located in the same directory as the matching VI. The installer will place this file in the LabVIEW addons directory along with the FPGA VI.

Connector Pane



Controls and Indicators

InpSig Signal to be measured for period and pulse width.

PulseCountTime Span of time during which rising edges are counted and reported in PulseCount.

PeriodAccumCount Number of pulses to accumulate periods to PeriodAccum.

StopValue When CurrentTime reaches StopValue, then Stopped is set to TRUE, and Period and PulseWidth are set to zero.

PPWAData Cluster of data reporting the measured parameters of the incoming InpSig.

- **Period** Period between the most recent rising edges of InpSig in terms of clock ticks. Period is reported as zero when Stopped is TRUE.
- **PulseWidth** Pulse width from the most recent rising edge to the most recent falling edge of InpSig in terms of clock ticks. PulseWidth is reported as zero when Stopped is TRUE.
- **PeriodAccum** Accumulation of periods over the specified number of pulses in PeriodAccumCount.
- **PulseCount** Number of rising edges counted over the specified time of PulseCountTime.
- **Stopped** Set to TRUE when StopValue is reached by CurrentTime.

CurrentTime Running clock ticks since the most recent rising edge of InpSig.

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InpSigROS Rising-edge one-clock one-shot of InpSig.

InpSigFOS Falling-edge one-clock one-shot of InpSig.

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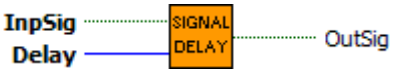
signal_delay_reva.vi

This VI outputs the same Boolean signal wired to the input, but with a Delay specified in 40MHz clock ticks.

This VI must be placed within a Single Cycle Loop (SCL) of a LabVIEW FPGA block diagram.

The FPGA VI requires a pre-synthesized netlist file having a matching name and an extension of .ngc. The netlist file must be located in the same directory as the matching VI. The installer will place this file in the LabVIEW addons directory along with the FPGA VI.

Connector Pane



Controls and Indicators

InpSig Input signal requiring a delay.

Delay Delay of the output rising and falling edges with respect to the input rising and falling edges, respectively, in terms of 40 MHz clock ticks.

OutSig Delayed version of the input signal.

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signal_extend_reva.vi

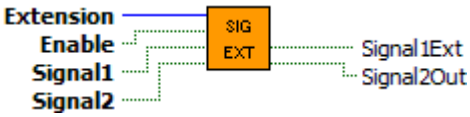
When enabled, Signal1 is extended (or possibly shortened) by the number of rising edges of Signal2 as specified by Extension and referenced to the rising edge of Signal1. Signal1Ext is the resulting output. Signal2Out is identical to Signal2. When disabled, Signal1Ext is identical to Signal1.

This VI is designed to accept a short single arbitrary cam pulse and extend it by a specified number of high-resolution crankshaft encoder pulses. The resulting extended cam pulse can be ANDed with the encoder index pulse so that only every other index pulse is sent to the Engine Position Tracking (EPT) VI.

This VI must be placed within a Single Cycle Loop (SCL) of a LabVIEW FPGA block diagram.

The FPGA VI requires a pre-synthesized netlist file having a matching name and an extension of .ngc. The netlist file must be located in the same directory as the matching VI. The installer will place this file in the LabVIEW addons directory along with the FPGA VI.

Connector Pane



Controls and Indicators

Extension Number of Signal2 pulses to extend Signal1.

Enable When TRUE, extension of Signal1 is enabled.

Signal1 Signal to be extended by a specified number of Signal2 pulses.

Signal2 Clock source of extending Signal1.

Signal1Ext The extension of Signal1.

Signal2Out Passthrough of Signal2.

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signal_offset_reva.vi

When enabled, Signal1 is offset by the number of rising edges of Signal2 as specified by Offset and referenced to the rising edge of Signal2 which immediately follows the rising edge of Signal1. Signal1Offset is the resulting output. Signal1Offset will go high at the falling edge of Signal2 immediately following the specified number of rising edges of Signal2. Signal1Offset will go low at the following rising edge of Signal2. Signal2Out is identical to Signal2. When disabled, Signal1Offset is identical to Signal1. When Offset is zero, Signal1Offset will remain low.

This VI is designed to offset or shift the index pulse of a crankshaft encoder by a specified number of high resolution encoder pulses. This eliminates the need to mechanically adjust the encoder for an exact alignment of the index pulse with respect to TDC. Proper alignment can be determined by monitoring cylinder pressure metrics.

This VI must be placed within a Single Cycle Loop (SCL) of a LabVIEW FPGA block diagram.

The FPGA VI requires a pre-synthesized netlist file having a matching name and an extension of .ngc. The netlist file must be located in the same directory as the matching VI. The installer will place this file in the LabVIEW addons directory along with the FPGA VI.

Connector Pane

Controls and Indicators

Offset Number of Signal2 pulses to offset Signal1.

Enable When TRUE, offset of Signal1 is enabled.

Signal1 Signal to be offset by a specified number of Signal2 pulses.

Signal2 Clock source of offseting Signal1.

Signal1Offset The offset of Signal1.

Signal2Out Passthrough of Signal2.

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