# VR Hall Module Kit User's Manual
## D000015 Rev B
**January 4, 2007**

Drivven ,Inc. • 12001 Network Blvd., Bldg. E, Suite 110 • San Antonio, Texas 78249 • USA
Phone : 210.248.9308
Web : www.drivven.com , E-mail : info@drivven.com

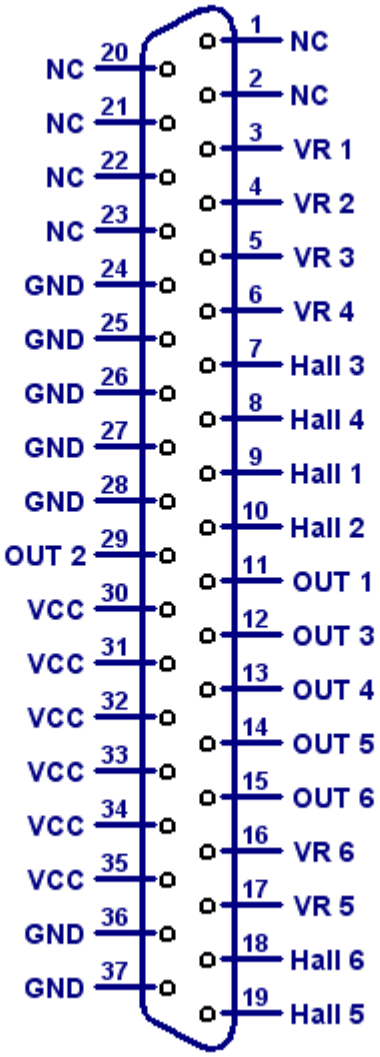
# Introduction

The Drivven VR/Hall Module Kit offers a set of automotive style inputs to interface with standard automotive sensors. It provides six channels which may be software selected as a VR sensor or hall-effect sensor input.

**Features:**

- 6 Ch. total, individually software-configured as VR or hall-effect sensor inputs
- 6 Ch. VR sensor inputs
  - +/-150 V input range
  - Adaptive threshold
- 6 Ch. Hall-effect sensor or general purpose digital inputs
  - Digital input with hysteresis
  - Over/under voltage protection
  - Optional Pullup, Pulldown, and Divide resistors
  - Analog filter for noise rejection
- External output for each channel according to software configuration
- Sensor power
  - 5V @ 100mA
  - Protected with resettable fuse

## Pinout


1 NC
2 NC
3 VR 1
4 VR 2
5 VR 3
6 VR 4
7 Hall 3
8 Hall 4
9 Hall 1
10 Hall 2
11 OUT 1
12 OUT 3
13 OUT 4
14 OUT 5
15 OUT 6
16 VR 6
17 VR 5
18 Hall 6
19 Hall 5
20 NC
21 NC
22 NC
23 NC
24 GND
25 GND
26 GND
27 GND
28 GND
29 OUT 2
30 VCC
31 VCC
32 VCC
33 VCC
34 VCC
35 VCC
36 GND
37 GND

# Hardware

This module provides six input channels which may be individually software selected as VR sensor input or hall-effect sensor input. It also provides sensor power and ground. Sensor power is provided directly from the cRIO chassis backplane. All sensors should not draw more than a total of 100mA. VCC pins are protected with a 0.1A resettable fuse.

Each of the six main channels provide an external output. The signal output is configured according to the software selection of VR or Hall.

A properly strain relieved DB-37 connector (not included) is used to interface to the module. National Instruments provides the "cRIO-9933 37-pin Conn. Kit, screw term conn. and DSUB shell" which is compatible with this module. However, any DB-37 connector system may be used. Drivven recommends the following DB-37 connector parts and tools available from Mouser at www.mouser.com.

Table 1. Connector parts list

| Description | Mfr.'s Part # | Mouser's Part # |
|---|---|---|
| AMP HDP-20 Series 109 37P Receptacle Housing | 1757820-4 | 571-1757820-4 |
| AMP HDP-20 Series 109 Crimp Socket Contact | 205090-1 | 571-2050901 |
| Norcomp D-Sub Connector Hood, 37P 45 Degree | 971-037-020R121 | 636-971-037-020R121 |
| AMP D-Sub Insert/Extract Tool | 91067-2 | 571-910672 |
| AMP Crimp Tool | 601966-1 | 571-6019661 |
| AMP Crimp Tool Pin Positioner | 601966-5 | 571-6019665 |

# Powering the Module

The VR/Hall module requires power from a single source.

The power source is from the CompactRIO backplane male high density D-Sub 15-pin (HD15) connector which mates with the module's female HD15 connector. This power source provides a regulated 5 volts and ground to various digital logic functions within the module. The CompactRIO 5V source is active whenever the CompactRIO or R-Series Expansion Chassis is properly powered. The module should only be powered at the HD15 connector by plugging it into a CompactRIO or R-Series Expansion Chassis. The module's HD15 connector should not be connected to any other device. The module may be inserted and removed at any time.

# Platform Compatibility

CompactRIO modules from Drivven are compatible within two different platforms from National Instruments. One platform is CompactRIO, consisting of a CompactRIO controller and CompactRIO chassis as shown in Figure 1a below.

Figure 1a. CompactRIO platform compatible with Drivven CompactRIO modules.

The other platform is National Instruments PXI which consists of any National Instruments PXI chassis along with a PXI RT controller and PXI-78xxR R-Series FPGA card. An R-Series expansion chassis must be connected to the PXI FPGA card via a SHC68-68-RDIO cable. The CompactRIO modules insert into the R-Series expansion chassis. This platform is shown in Figure 1b below.

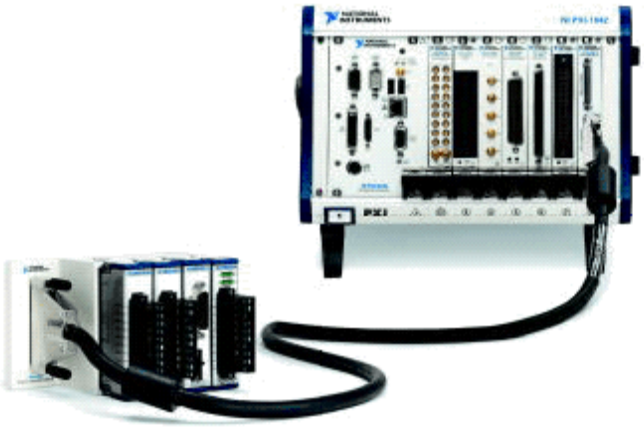


Figure 1b. PXI platform compatible with Drivven CompactRIO modules.

Drivven CompactRIO modules are not compatible with the National Instruments CompactDAQ chassis.

Drivven CompactRIO modules REQUIRE one of the hardware support systems described above in order to function. The modules may not be used by themselves and/or interfaced to third party devices at the backplane HD15 connector. These efforts will not be supported by Drivven or National Instruments.

## VR Sensor Inputs

The VR Hall module provides up to six identical VR sensor inputs. A Variable Reluctance (VR) sensor input is a standard low cost automotive speed sensing input. It is an electro-magnetic sensing device containing a winding of wire around a permanent magnetic core. It relies on the movement of ferrous material (steel teeth) past the tip of the sensor to change the magnetic flux of the sensor. This creates a voltage pulse across the leads of the sensor's wire coil. Figures 4 and 5 below show a typical VR signal with respect to toothed wheels, as shown in figures 2 and 3. The VR signal will go positive as a tooth approaches the sensor tip. The signal will then rapidly swing back through zero precisely at the center of the tooth. As the tooth moves away from the sensor tip the voltage will continue in the negative direction and then return to zero.

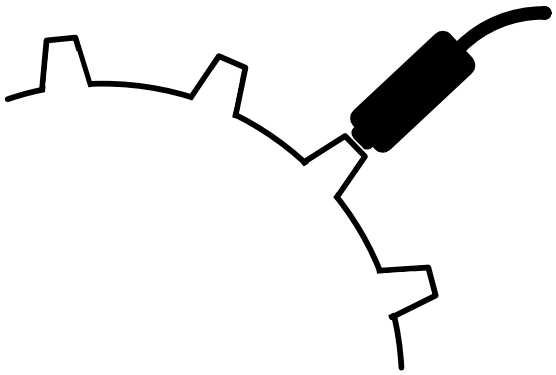


Figure 2. Positive tooth trigger wheel

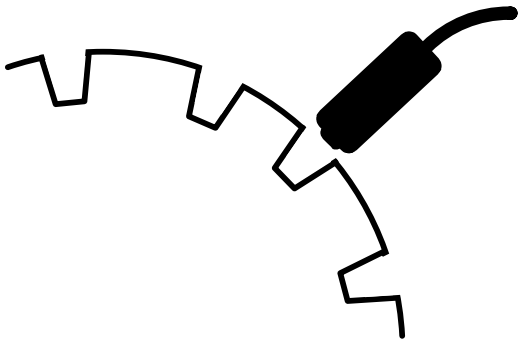


Figure 3. Negative tooth trigger wheel

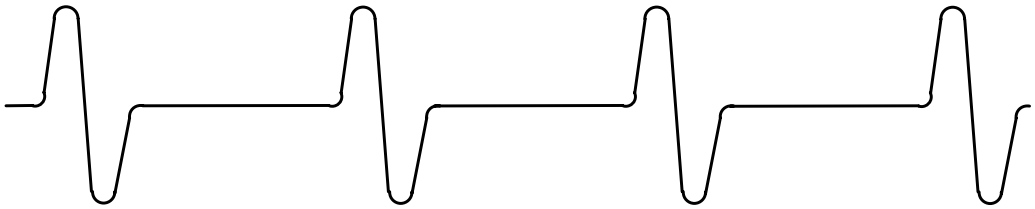


Figure 4. Correct signal polarity for VR input circuit

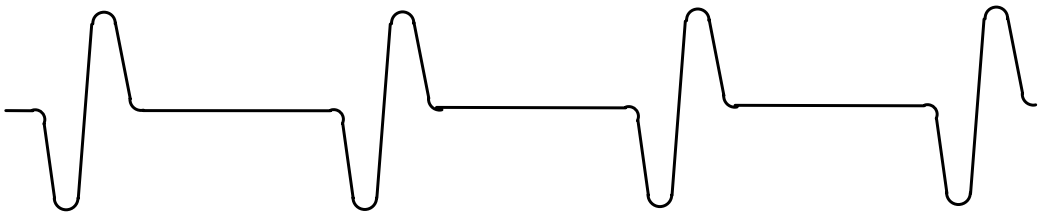


Figure 5. Incorrect signal polarity for VR input circuit

Each VR sensor input requires two connections. The VR Hall module pins labeled VR1 thru VR6 are the positive sensor inputs. The negative sensor inputs must be connected to GND pins on the module. The polarity of the sensor connection to the module is critical. The leads of the sensor should be connected such that the positive input of the VR circuit sees the waveform shown in Figure 4. The waveform shown Figure 5 is incorrect, and the VR circuit will not properly respond to this waveform. The rapid zero crossing of the VR signal must be in the negative direction.

The polarity of the physical tooth or gap on the trigger wheel will contribute to the polarity of the voltage pulse from the sensor. Figure 2 demonstrates a positive physical tooth polarity and Figure 3 demonstrates a negative physical tooth polarity. Assuming the lead polarity of a sensor remained the same, one of the configurations would generate the waveform shown in Figure 4, while the other configuration would generate the waveform shown in Figure 5.

Triggers wheels are designed so that the physical center of each tooth or gap corresponds to a known angular position of the wheel. This physical center of the tooth or gap always corresponds to the rapid zero-crossing of the generated voltage pulse.

The VR circuit is designed so that the rapid negative zero-crossing of the raw sensor signal corresponds to the rising edge of a digital pulse sent to the RIO FPGA. The VR output signal to the FPGA will go TRUE at the rapid negative zero crossing of the external VR pulse and remain TRUE until the external VR pulse returns to 0V. An example of this is shown in Figure 6. Within LabVIEW FPGA the system designer can route this digital signal to the EPT CrankSig or CamSig input. The signal can also be routed to any other speed measurement sub-VI.

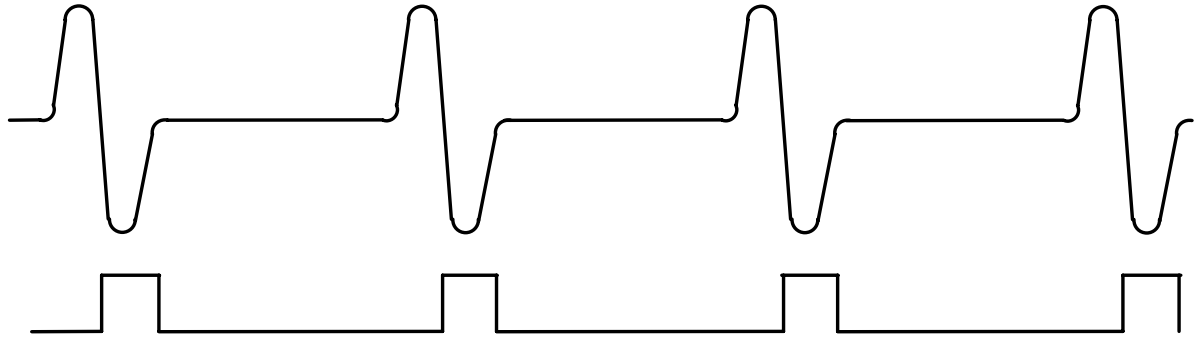


Figure 6. VR input pulse and resulting digital output from VR circuit

The absolute maximum VR pulse amplitude allowed by the circuit is +/-150 volts. If the input signal exceeds this voltage, damage may occur to the circuit. The amplitude should not exceed +/-150 volts at maximum engine speed. The minimum VR pulse amplitude that will generate a digital output by the VR circuit is +/-200 millivolts.

The VR circuit implements adaptive noise rejection features during continuous incoming VR pulses. In general, an adaptive arming threshold voltage is generated with each VR pulse and bleeds down thereafter. The next pulse must have an amplitude that exceeds the arming threshold in order for a digital output to be generated at the rapid zero-crossing. The initial arming threshold is set to approximately 70% of each pulse's amplitude.

Given a constant gap between the sensor and the trigger teeth, the amplitude of a VR pulse is directly proportional to the speed of the trigger wheel. For example, if the VR amplitude at 1000 RPM is +/-10 volts, then the amplitude at 2000 RPM will be +/-20 volts. By using an oscilloscope to measure the VR amplitude at a low speed, this relationship can be used to determine what the maximum amplitude will be at the maximum speed. If the maximum amplitude of +/-150 volts will be exceeded at maximum speed, then the sensor gap must be increased, or the designer must obtain a custom VR circuit configuration from Drivven.

## Hall-Effect Sensor Inputs

The VR Hall module provides up to six identical hall-effect sensor input circuits. The hall-effect inputs are designed to take a digital input from a hall-effect or proximity sensor. Typical sensors of this type will have an open-collector output, requiring a pullup resistor at the collector. The hall-effect inputs will also read active TTL compatible signals. The standard configuration includes a 4.7K pullup to 5V for use with open collector type inputs. The input is protected against typical automotive battery voltages and can be connected to actively-driven, battery voltage signals. Channels with this configuration are protected from voltage swings of -4V to +14V.

The circuit's output to the RIO FPGA reverses the polarity of the input by going low when the input voltage is greater than 2.0V. The output goes high when the input is less than 1.0V. The input hysteresis requires the input to move all the way to the opposite logic level before the output changes.

Figure 7 shows the standard configuration of the hall-effect sensor input circuits.

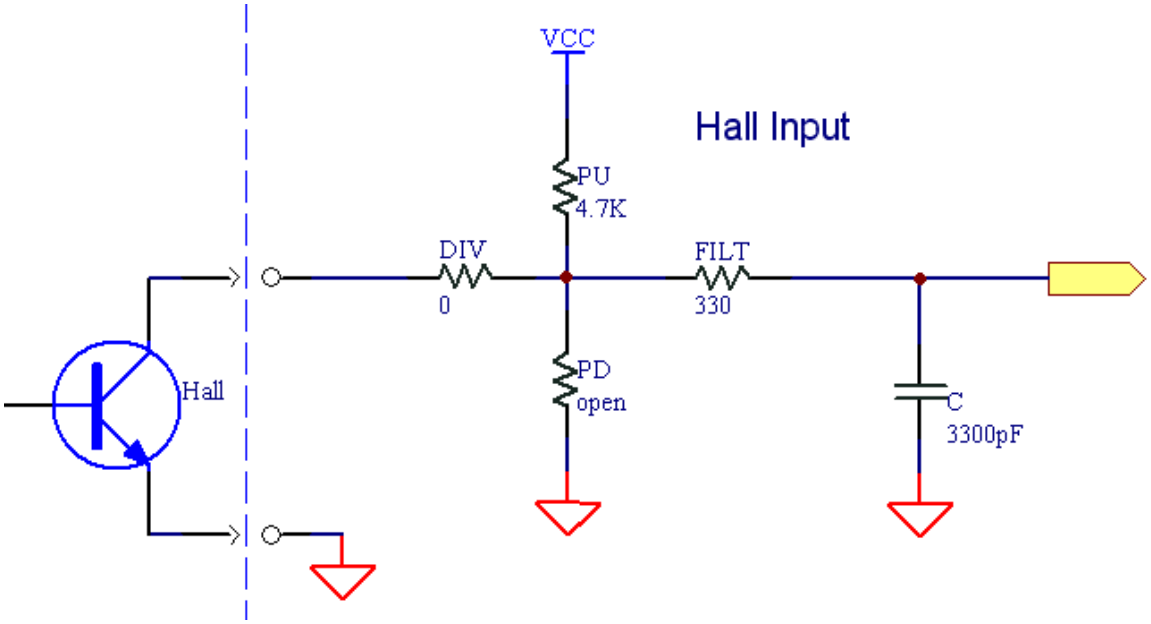



Figure 7. Hall-effect circuit input configuration

# Software

The VR/Hall Module Kit is provided with a LabVIEW FPGA VI for interfacing to the module and reporting VR and hall signal results.

Figure 8 shows the icon which represents vr_hall.vi.

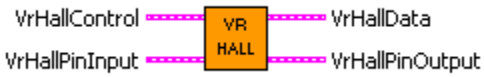



Figure 8. vr_hall_revx.vi icon with leads.

**VERY IMPORTANT NOTES:**

The FPGA VI requires:

- LabVIEW 8.2 Full Development or later
- LabVIEW RT Module 8.2 or later
- LabVIEW FPGA Module 8.2 or later
- NI-RIO 2.1 or later

The FPGA VI must be placed within a Single Cycle Loop (SCL) of a LabVIEW FPGA block diagram. The SCL must execute at the default clock rate of 40 MHz.

The FPGA VI requires a pre-synthesized netlist file having a matching name and an extension of .ngc. The netlist file must be located in the same directory as the matching VI.

The FPGA VI requires the installation of a special CompactRIO module support package called cRIO-generic. Please follow the steps below to install the cRIO-generic package:

1. Confirm that LabVIEW is closed.
2. Add the line **`cRIO_FavoriteBrand=generic`** to the LabVIEW INI file. The LabVIEW INI file is typically found at C:\Program Files\National Instruments\LabVIEW 8.0\LabVIEW.ini.
3. Upon restarting LabVIEW, the cRIO-generic module will appear in the list of available modules within the LabVIEW FPGA "New C Series Module" configuration dialog. All Drivven CompactRIO modules require adding an associated cRIO-generic module to your LabVIEW Project. Within the Project Explorer, A cRIO-generic module can be added to a PXI FPGA expansion chassis or a CompactRIO chassis. This is best understood by observing an example project provided with your module kit.

**WARNING!**

When writing values to an FPGA cluster from the RT level, every parameter within the cluster must be explicitly written. If any parameter is not explicitly written, then the default value for that particular data type will be used. This could cause unexpected behavior.

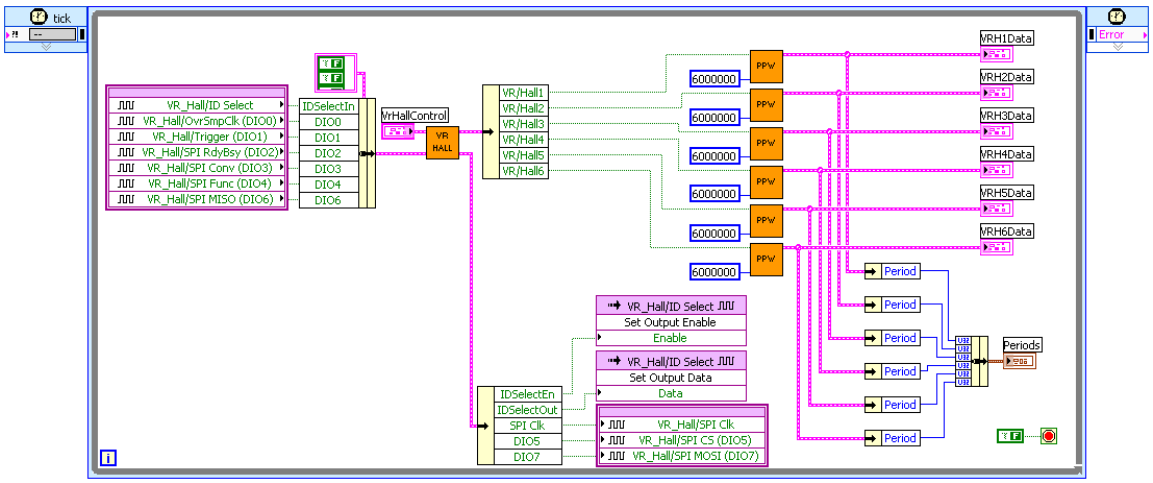



Figure 9. Example block diagram implementation of vr_hall_revx.vi.

**VRHallPinInput** (Cluster)
These boolean controls must be connected to their corresponding FPGA I/O Node input item.

**VRHallPinOutput** (Cluster)
The boolean indicator named IDSelectEn must be connected to a Set Output Enable method of an FPGA I/O Method Node. The boolean indicator named IDSelectOut must be connected to a Set Output Data method of an FPGA I/O Method Node. The remaining boolean indicators must be connected to their corresponding FPGA I/O Node output item.

**WARNING!**
Great care must be taken to ensure that LabVIEW FPGA I/O node output items are only wired from a single logic source. There is no circumstance in which FPGA I/O node output items should be driven by multiple sources when interfacing to cRIO modules, otherwise strange behavior or module damage could result. Two LabVIEW FPGA code snippets are shown below which illustrate this issue. Figure 10a shows the correct implementation of FPGA I/O node blocks, whereas a group of three outputs to an ADCombo module are controlled while another group of eight outputs to a Spark module are controlled. Each of the output items are selected only once in the entire block diagram. On the other hand, figure 10b shows a coding mistake that should be avoided. Notice the group of ADCombo output items where a Spark module output item is selected instead of the correct ADCombo module output item. The same Spark module output item is also selected in the Spark group below. This means that the Spark (DIO5) output is being driven by two different logic sources and will cause strange behavior of the spark module, or possible damage.

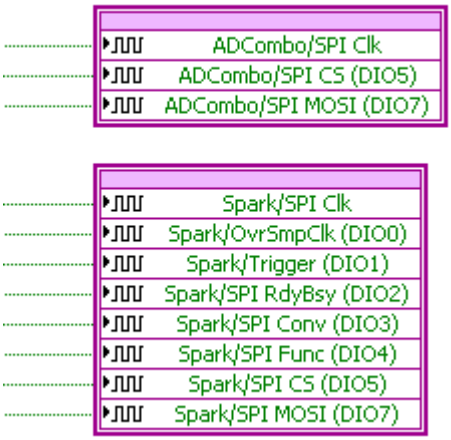



Figure 10a. Representative FPGA output nodes for ADCombo and Spark modules with correct output item selection.

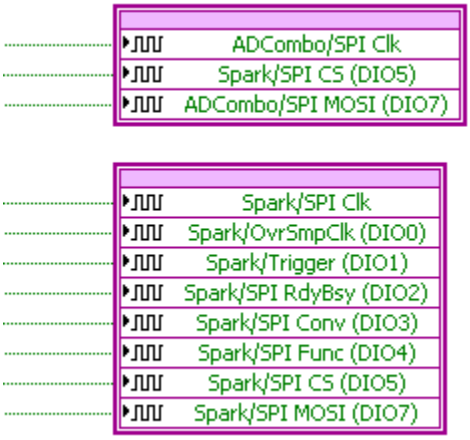



Figure 10b. Representative FPGA output nodes for ADCombo and Spark modules with incorrect output item selection within the ADCombo output node. The Spark (DIO5) output is selected in multiple nodes and therefore being driven by multiple sources. This will cause strange behavior or damage to the spark module.

One way to help prevent such coding mistakes is to prefix all FPGA I/O item names with an appropriate unique module name via the FPGA I/O creation dialog or via the project explorer, after the I/O item is created. This will make the coding mistake recognizable from the block diagram. Another way this situation can be prevented, even when a coding mistake is made, is by making sure that all FPGA output node items are configured to "Arbitrate if Multiple Accessors Only." When outputs are configured this way and they are used within a Single Cycle Loop (as is required by Drivven cRIO module kits), then a compile error will be generated if multiple sources are driving FPGA output node items. Then appropriate corrective action can be taken. FPGA output node items can be configured via the FPGA I/O properties dialog, by right clicking on the FPGA I/O item within the project explorer. FPGA output node properties should be set according to the following dialog screen shot.

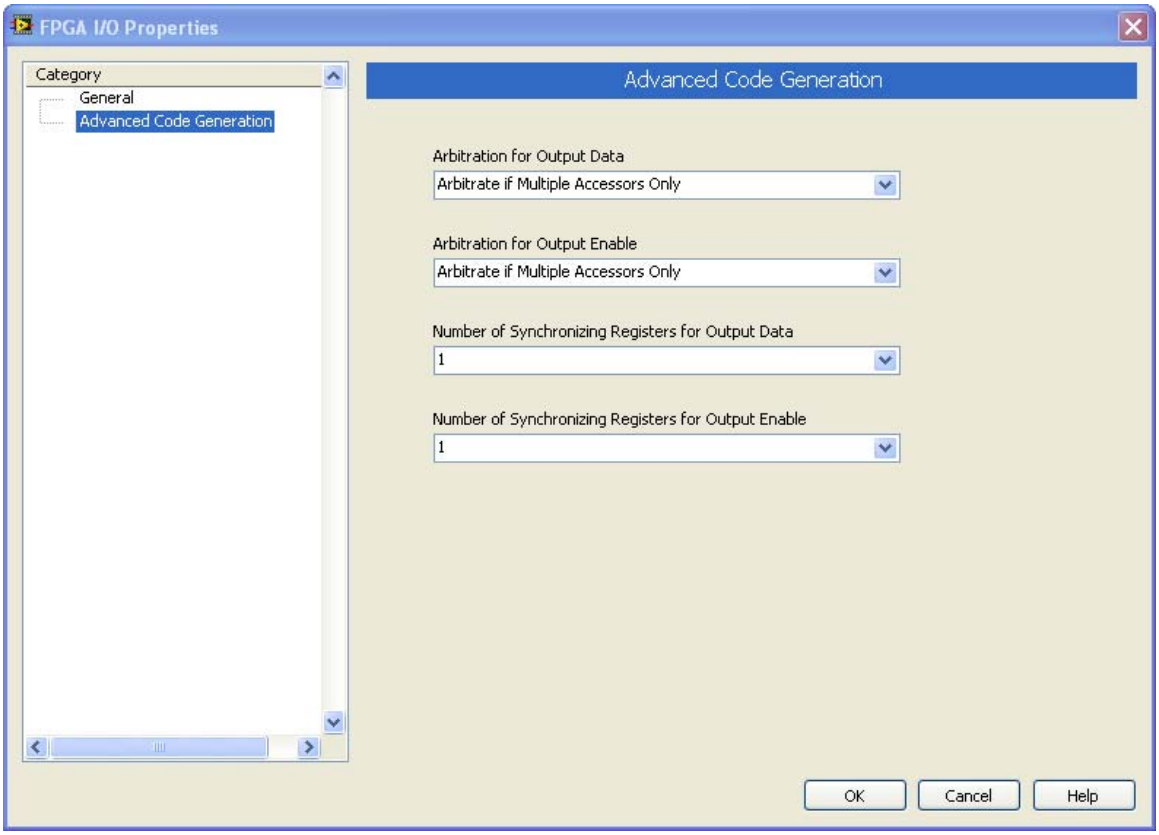
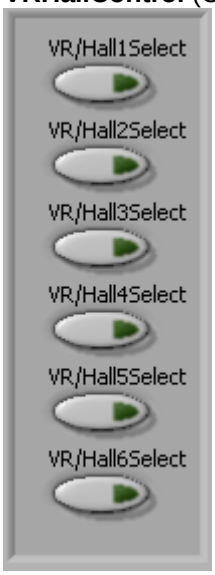



Figure 11. FPGA I/O Properties dialog configuration for cRIO modules.

**VRHallControl** (Cluster)




**VR/HallXSelect (boolean):** When FALSE the input channel is selected as a VR sensor input. When TRUE, the input channel is selected as a hall-effect sensor or general purpose digital input.

**VRHallData** (Cluster)


**VR/HallX (boolean):** When selected as a VR sensor input, the VR/Hall output signal will go TRUE at the rapid negative zero crossing of the external VR pulse and remain TRUE until the external VR pulse returns to 0V. It is important to only use the rising edge of this digital signal because it is always lined up with the rapid negative zero crossing of the external VR pulse. When selected as a hall-effect sensor or general purpose digital input, the VR/Hall output is an inverted and filtered version of the external signal presented to the hall-effect input channel. The external output pins also reflect the same signal as presented to the RIO FPGA.

# Standard Circuit Configuration

The VR/Hall module is hardware-configurable. It may be ordered with the default options outlined below or may be custom ordered. It may not be configured by the user.

**Standard VR Configuration**

| Channel | VR Amplitude Voltage |
|---|---|
| 1 | +/- 150V |
| 2 | +/- 150V |
| 3 | +/- 150V |
| 4 | +/- 150V |
| 5 | +/- 150V |
| 6 | +/- 150V |

**Standard Hall Configuration**

| Channel | Pullup Resistor (ohms) | Pulldown Resistor (ohms) | Divide Resistor (ohms) | Break Frequency (Hz) | Intended Use |
|---|---|---|---|---|---|
| 1 | 4.7k | open | 0 | 150K | Hall, Prox, Switch or TTL |
| 2 | 4.7k | open | 0 | 150K | Hall, Prox, Switch or TTL |
| 3 | 4.7k | open | 0 | 150K | Hall, Prox, Switch or TTL |
| 4 | 4.7k | open | 0 | 150K | Hall, Prox, Switch or TTL |
| 5 | 4.7k | open | 0 | 150K | Hall, Prox, Switch or TTL |
| 6 | 4.7k | open | 0 | 150K | Hall, Prox, Switch or TTL |

# Custom Configuration

For an additional service charge, Drivven will custom configure each VR and/or Hall chanel. Customization can take place during or after module purchase.

When requesting a custom configuration please provide all of the following information.

| | |
|---|---|
| **Customer Business Name** | |
| **Contact Name** | |
| **Contact Phone** | |
| **Contact Email** | |
| **Shipping Address** | |
| **Unit Serial Number** | |
| **Has this unit been modified by the user?** | |

| Channel | Pullup Resistor (ohms) | Pulldown Resistor (ohms) | Divide Resistor (ohms) | Break Frequency (Hz) | Intended Use |
|---|---|---|---|---|---|
| **Hall 1** | | | | | |
| **Hall 2** | | | | | |
| **Hall 3** | | | | | |
| **Hall 4** | | | | | |
| **Hall 5** | | | | | |
| **Hall 6** | | | | | |

| Channel | VR Amplitude Voltage |
|---|---|
| **VR 1** | |
| **VR 2** | |
| **VR 3** | |
| **VR 4** | |
| **VR 5** | |
| **VR 6** | |

# Examples

The following screen capture in Figure 12 shows a LabVIEW FPGA block diagram with the VR/Hall VI used for general purpose speed measurement. The VR/Hall signals may also be routed to the CrankSig and CamSig inputs of Drivven's EPT VIs for engine position tracking. This FPGA application is entirely contained within a single cycle loop, clocked at the required 40 MHz. The PinInput and PinOutput clusters are wired to LabVIEW FPGA I/O pins which are configured for a cRIO controller chassis or a cRIO R-Series expansion chassis. Refer to the LabVIEW FPGA documentation for details about configuring cRIO I/O pins.

This example VI is included in the VR/Hall Module Kit VI software bundle.

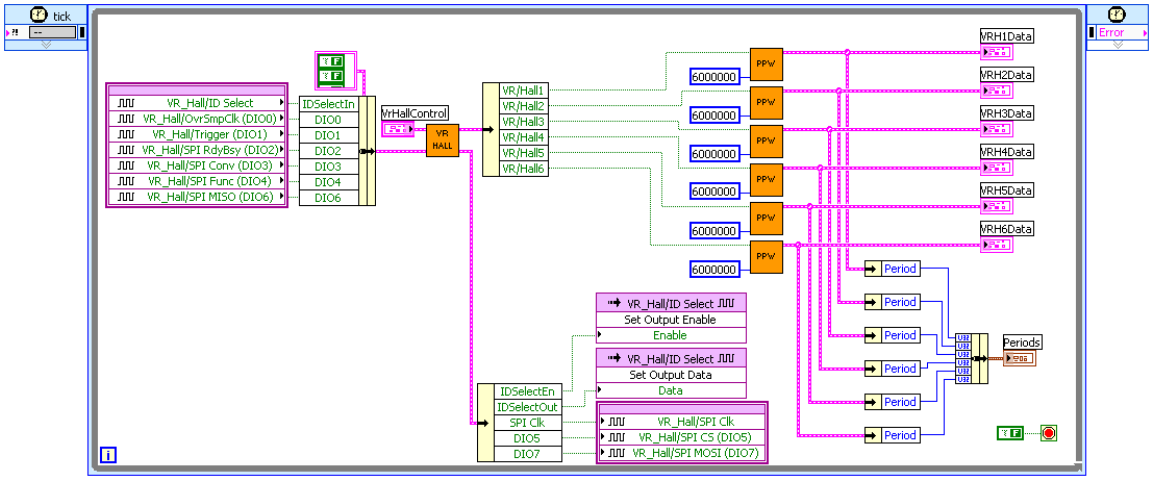



Figure 12. LabVIEW FPGA Block diagram example.